REMARKS

In the Office Action the Examiner did not indicate consideration of the drawing changes submitted with a response to the previous Office Action on December 30, 2003. However, in preparing a current response the originally filed drawings have been carefully reviewed and put in conformance with the specification. Reference numbers have been added to the drawings as described in the specification in order to clarify the claimed subject matter. For instance, the structure referred on the page 4, paragraph [0021] of the specification as a patterned resist 18 had not beenspecifically identified on the drawings. Now, the patterned apertures in the resist are given a reference number 18 on Figure 1. Additionally, the Figure 5B, showing a cross-sectional view orthogonal to Figure 5A and extending in the channel region introduced by the previous response, has been included with this amendment. The Examiner is respectfully requested to consider the proposed drawing corrections and provide an indication of such consideration in the next office action.

The specification has been carefully reviewed and minor corrections have been performed by this amendment mostly to add necessary reference numbers helpful for understanding the present invention. Additionally, the description of Figure 5B has been added to the list of the drawings on page 3 of the specification. No new matter has been added by this amendment. Responding to the Examiner's objection of limitation related to sub-lithographic dimensions, this limitation has been taken out of claim 1 and presented in the dependent claim 19. In regard of the definition of the term "sub-lithographic", the current level of optical lithographic techniques for producing nanoscale structures is reaching a fundamental limit of roughly 200 nm. The Applicant would like to point out that the definition of the term "sub-lithographic" is a term well-established and accepted in the art at the present time has feature sizes that is less than a lithography limit for a particular device and related to structures with dimensions less than 100 nm. However, the width, presented by the Applicant, is within approximately 5 nm to 50 nm as described in paragraph [0006] on page 1 of the

specification. This limitation has been presented in new claim 19 according to the present amendment.

Claims 1 to 8 and 19-22 are currently active in the application. By the present amendment claim 1 has been amended to clarify the claimed structure. Additionally, new claims 19 to 23 have been added for the Examiner's consideration. Support for new claims 18-22 is found on at least pages 7 to 9 of the present specification and Figures 5, 5A. No new matter has been introduced by this amendment.

Claims 1 to 3 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Mizuno et al. (U.S. Patent 5,844,278) in view of Sung (U.S. Patent ,792,690). This rejection is respectfully traversed for the reason that the combination of Mizuno et al. and Sung fails to show the invention as presently claimed.

The present invention aims to resolve the problems which take place in field effect transistors with channel or gate length below 50 nanometers. The previously proposed two gates structure of FET, however, can be optimal only if the two gates are self-aligned and have such a silicon thickness to gate dimension ratio that a device does not suffer from increased gate to junction capacitance. Therefore, the present invention provides a appropriate gate thickness in order to avoid gate to junction capacitance and reduced source to drain resistance. In addition, according to the present invention the conduction channel comprises monocrystalline structures which can guarantee uniform electrical characteristics of the device in whole.

The reference to Mizuno et al. is directed to formation of a transistor with a substrate having a semiconductor element region of a projection shape. The reference to Mizuno et al. aims to resolve several problems existing in a conventional projection-shaped transistors. Particularly, the problems are: width of channel, low control by a gate electrode the region of the projection , which is not covered with the gate electrode and control of the region located deeper than the projecting region surrounded by the gate electrode. Structurally, the device

proposed by Mizuno et al. comprises a substrate with a semiconductor element region of a projection shape, a gate electrode formed on an upper and side surfaces of the element region via a gate insulation film and source and drain regions, provided so as to form a channel region on the upper surface of the element region in such a manner that the gate electrode is interposed between the source region and the drain region. Generally, Mizuno et al., is specifically concerned about width of the element region and shows that a width W of the element region should satisfy the following equation:

$$W \leq 2\sqrt{2}\,(\epsilon_s \Phi_F / qN_{sub})^{1/2},$$

where q is an electron charge, Φ_F represents a Fermi level of the semiconductor substrate, ϵ_s is a dielectric constant of the semiconductor substrate and N_{sub} is an impurity concentration of the semiconductor substrate. Mizuno et al states that by setting the width W of the element region in a manner to satisfy the above equation, all the channel region is depleted. Specifically, describing one of the embodiments of the invention Mizuno et al. states that the width of the projecting region could be around *0.1 μm = 100 nm.* (See column 14, lines 26-30).

In contrast, the transistor device taught by Applicant belongs to the different type of Field Effect Transistor (FET) which has a dual gate comprising separated gate electrodes. The dual gate transistors have the several problems due to structural peculiarity. For instance, in order to provide an optimal performance the two gates should be self-aligned. However, this structure has an advantage over the taught by Mizuno et al., the semiconductor device with a projection-shaped semiconductor, wherein a gate structure wraps around the conduction channel. In Mizuno et al., the entire gate can only be driven to a single voltage even though it is desirable in some circumstances to place different voltages on opposite sides of the conduction channel.

Summarizing the above discussion the Applicant is respectfully submits that there are significant structural differences between the claimed device and the structure proposed b the primary reference to Mizuno et al. Specifically, the claimed device and structure to Mizuno et al. belongs to the different types of

semiconductor devices. The present invention is a dural-gate field effect transistor and Mizuno et al. discloses a semiconductor device with a projection-shaped semiconductor region. The both devices intend to reduce a conductor channel width, but if Mitzuno et al. in order to do that sets the width of the projection-shaped element region, the Applicant forms a mocnocrystalline sub-lithographic dimensions conductive channel between two gates structures.

To emphasize the distinction, claim 1 have been amended and new claims 18 to 22 have been added. Specifically, the amended claim 1 now recites, " . A field effect transistor with a dual-gate, comprising:

a monocrystalline conduction channel of a first width and a dual-gate of 100 mm or less,

source and drain regions located at opposite ends of said monocrystalline conduction channel, said source and drain regions having silicide sidewalls on a surface thereof wherein source-drain resistance is reduced, and

self-aligned polysilicon gate regions on opposing sides of said monocrystalline conduction channel and recessed from said source and drain regions wherein gate-junction capacitance is reduced, said polysilicon gate regions having silicide sidewalls formed thereon,

wherein the smallest feature of said field effect transistor formed through a lithographic process is of a second width, wherein said first width is smaller than said second width." (Emphasis added)

Furthermore, the Examiner relies on the reference to Sung as disclosing the silicide spacer. The reference to Sung discloses a process of fabrication of Dynamic Random Access Memory (DRAM) wherein space can be reduced by stacking the capacitor and transistor structures. Sung resolves the problem of aligning vertically the basic elements of DRAM: a word line transistor and a storage capacitor, occupying the same semiconductor substrate space. The vertical alignment of these elements will allow a DRAM cell which is equal to about eight times the minimum feature used, referred as $8F^2$. Sung also proposes to use a silicide spacer on the sides of the polysilicon gate structure in order to reduce gate

resistance. However, the Applicant claims a plurality of gate polysilicon regions having silicide sidewalls formed thereon which is as previously was noted having the lithographic dimensions. Specifically, Sung in column 5, lines 5-8 and in column 4, lines states that a size of channel 14C has a width 1500 Å to 2000 Å= 150 nm to 200 nm and length about 0.30 μm to 0.40 μm= 300 nm to 400nm. As it can be seen all structures in Sung have lithographic dimensions and therefore is not relevant to the present invention related to sub-lithographical structures.

Regarding to rejected claims 2, 3, 4 - 8 it is respectfully submitted that those claims are dependent from currently amended claim 1 and therefore are allowable.

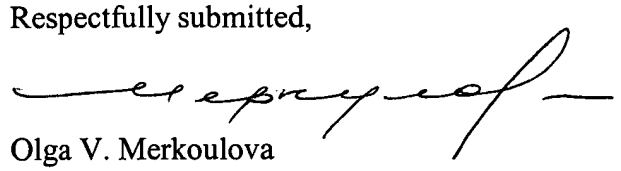
Rejecting claims 6 to 8, the Examiner relies on the reference to Liu et al. as disclosing a silicide sidewalls connected with a damascene connector formed within a trench in the insulation region. This rejection is respectfully traversed for the reason that the patent to Liu et al. also relates to the larger scaled devices and is not relevant to the present invention.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1 - 8, 18 to 22 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,



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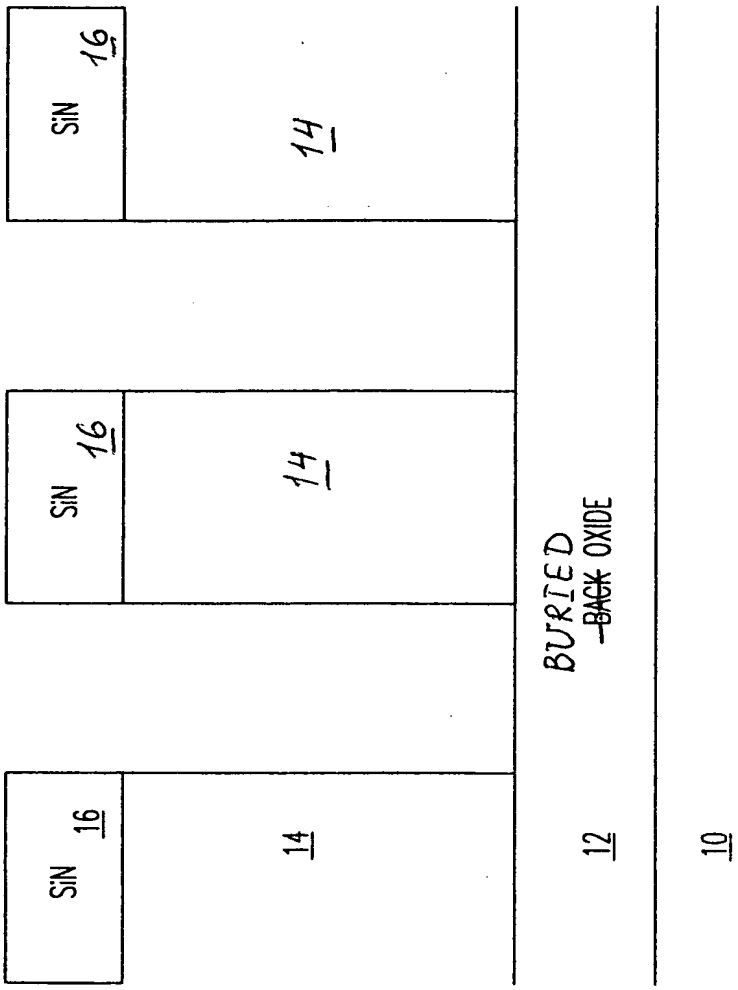

FIG. 1
(SECTION AA')

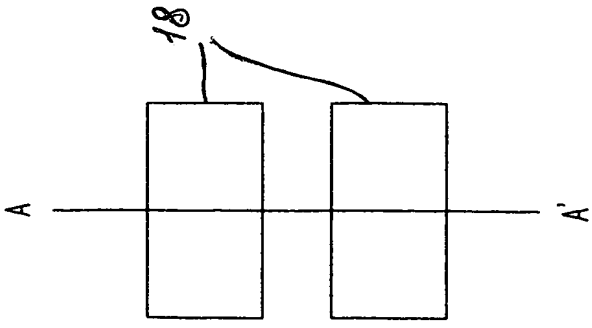

FIG. 1A

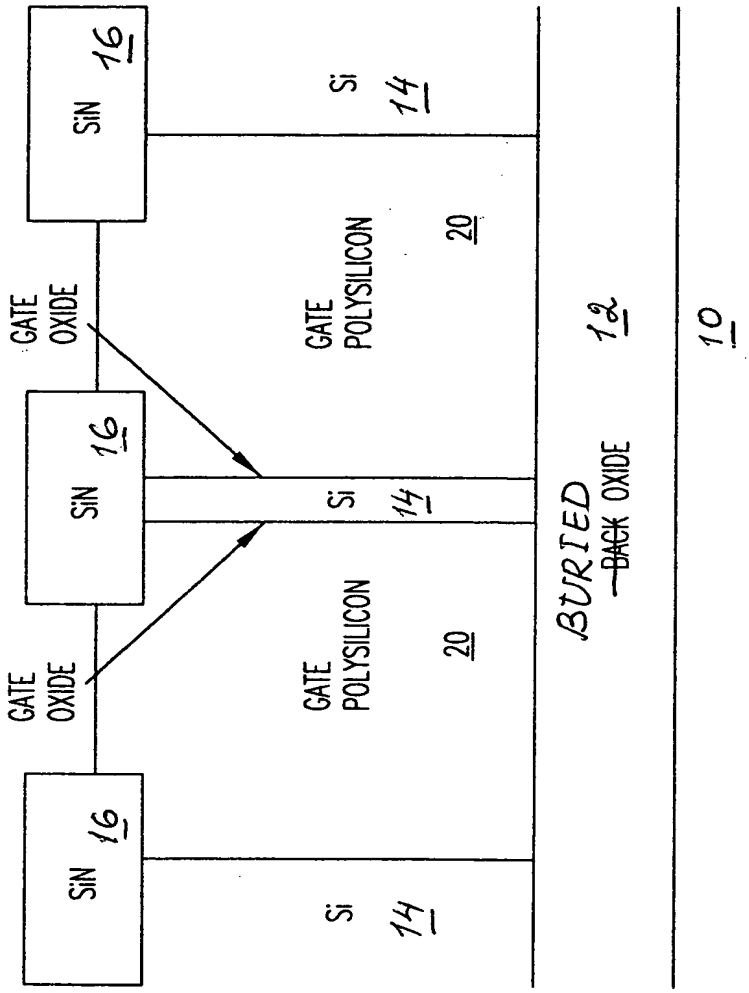

FIG. 2
(SECTION AA')

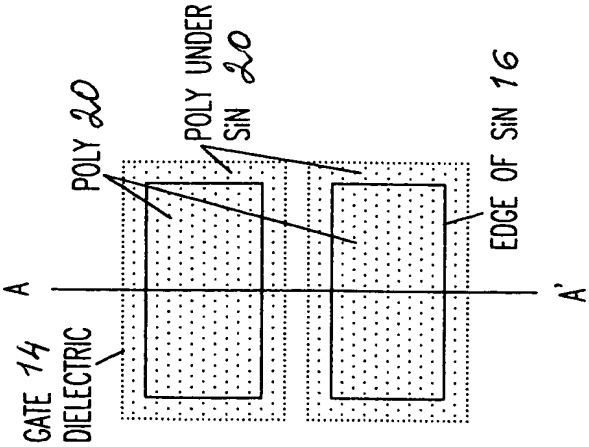

FIG. 2A

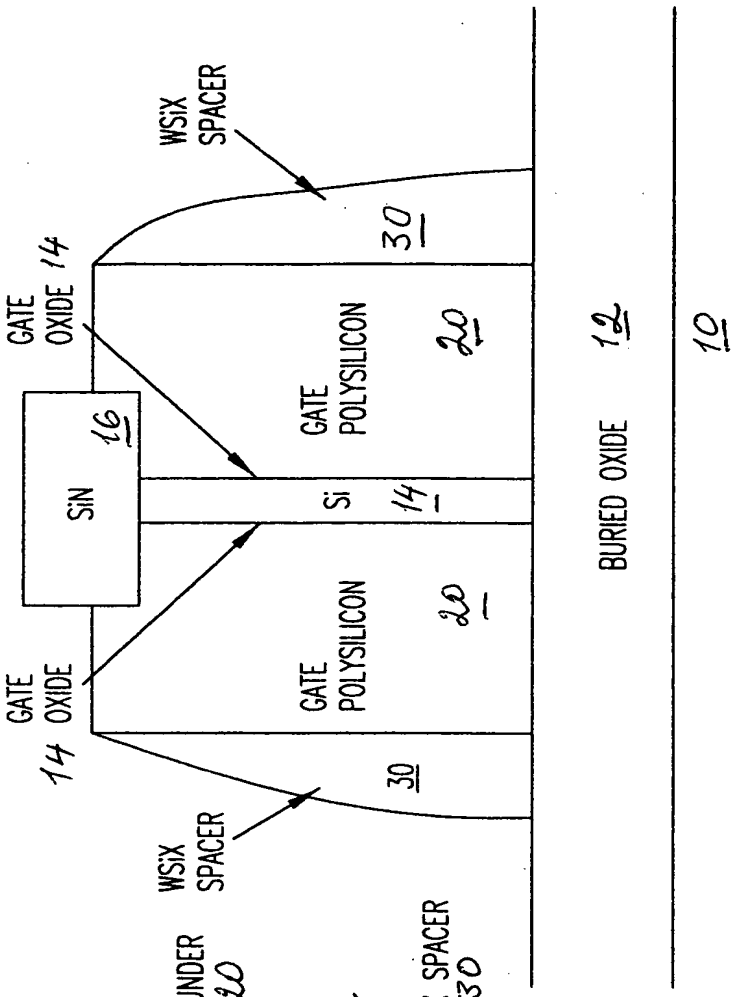

FIG. 3
(SECTION AA')

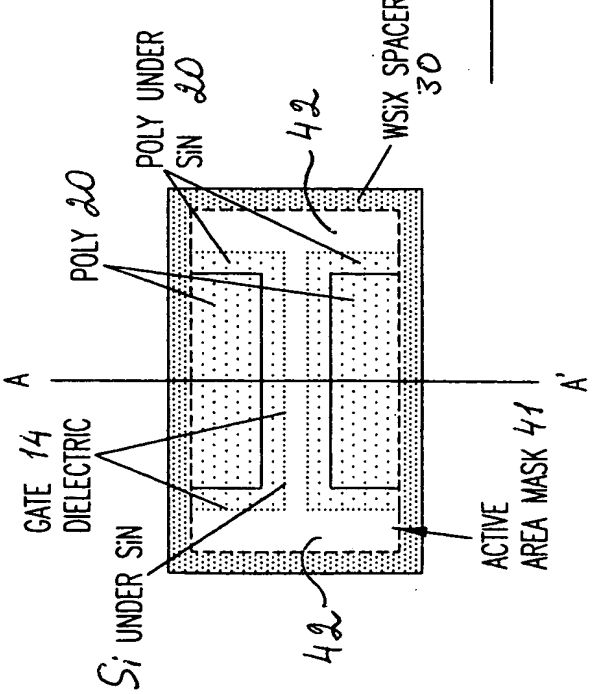

FIG. 3A

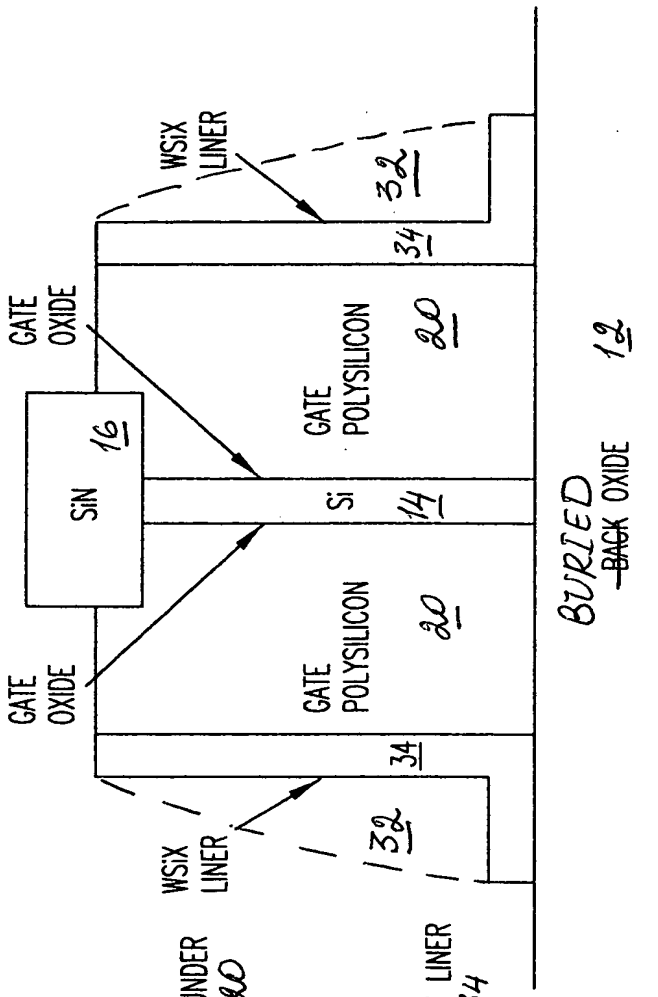

FIG. 3B
(SECTION AA')

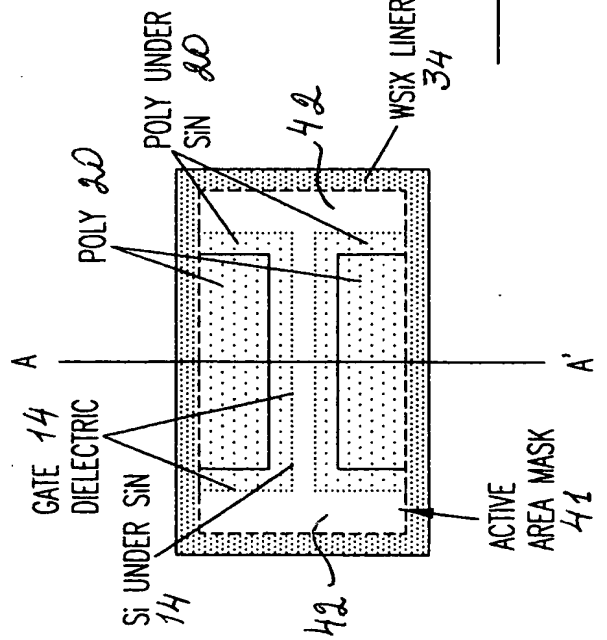

FIG. 3AB

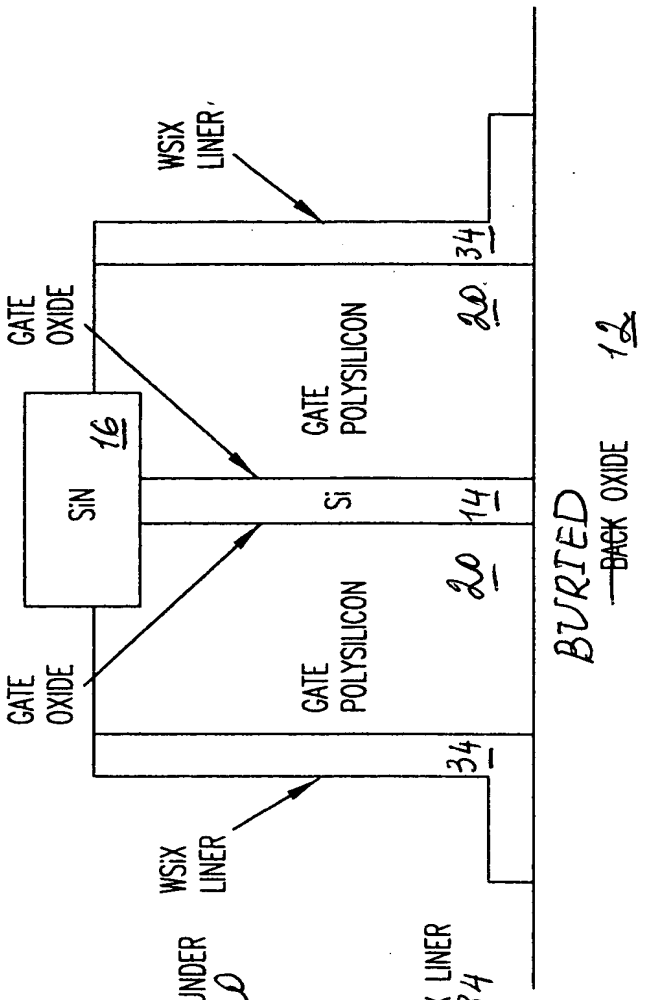

FIG. 4
(SECTION AA')

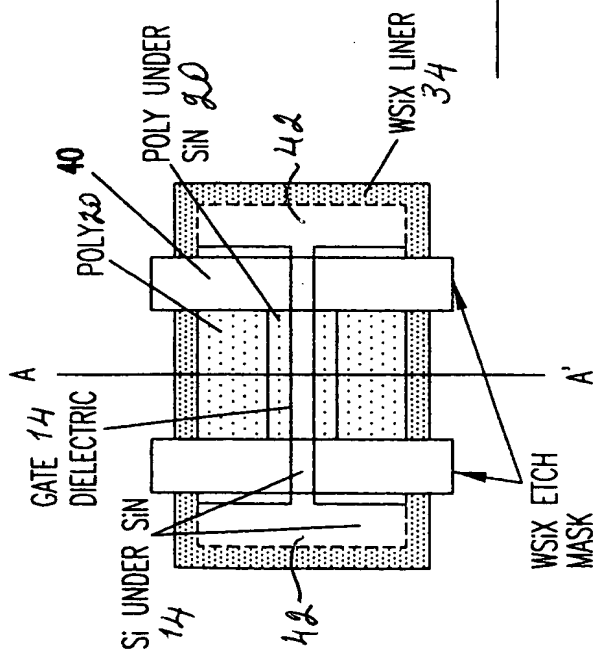

FIG. 4A

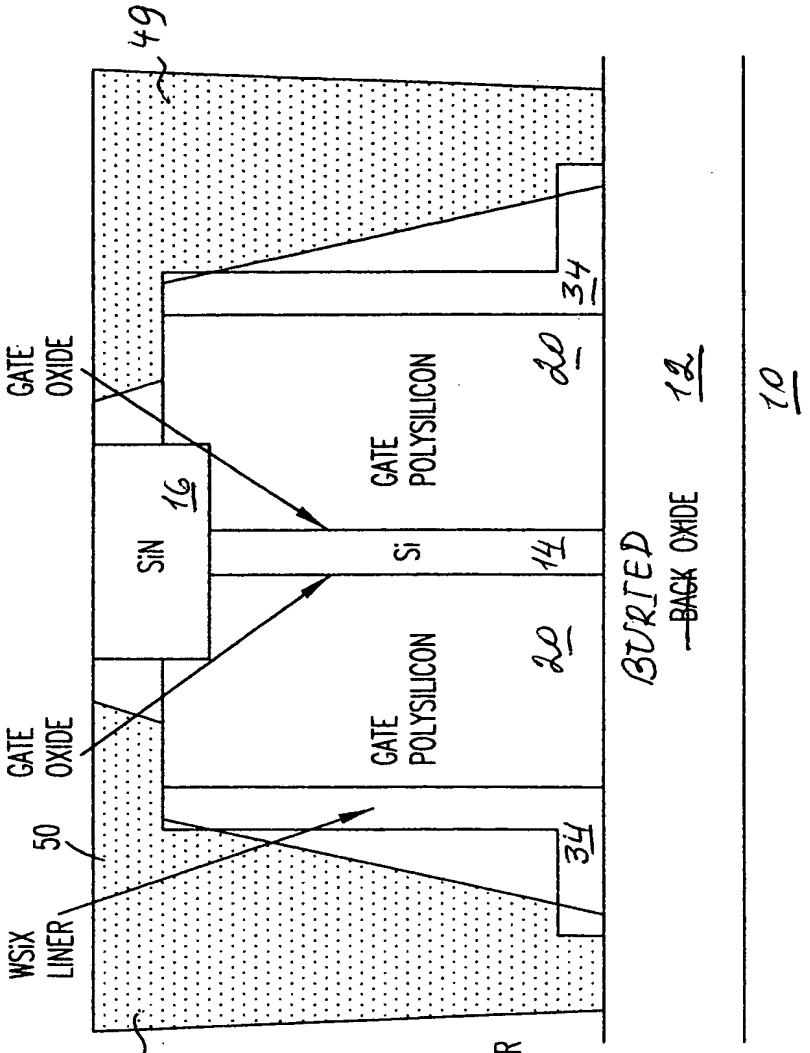

FIG. 5
(SECTION AA')

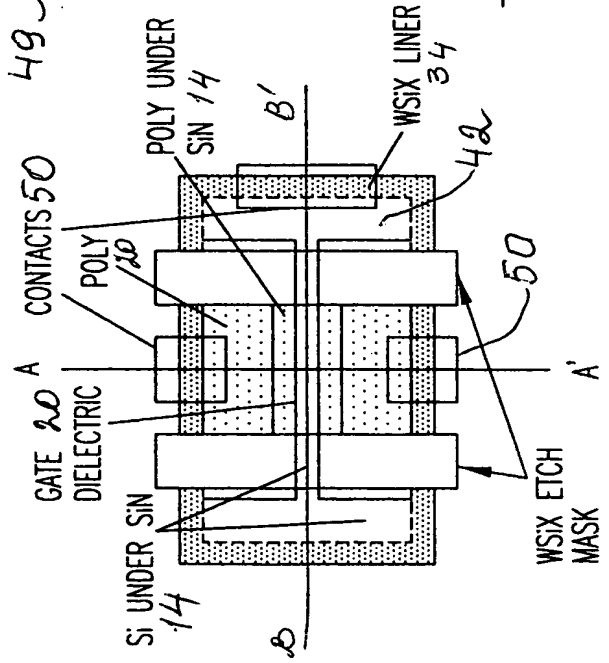

FIG. 5A

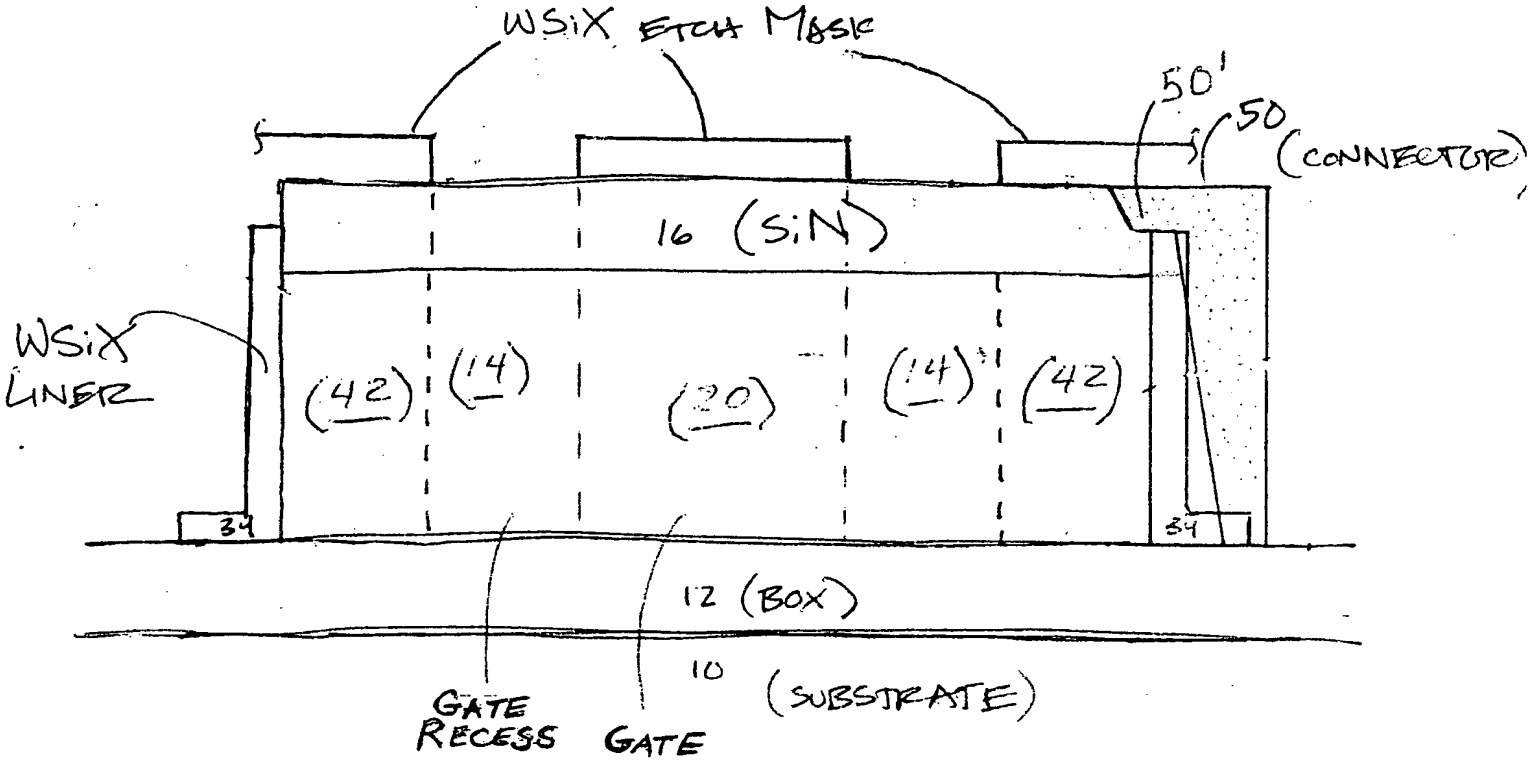

FIG. 5B (section BB')